a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion;

a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, thereby applying said write voltages only to memory cells which are not sufficiently written to achieve a predetermined written state.

64. The device according to claim 63, wherein said data stored in said programming circuits are initially set to initial data, and then said initial data stored in said programming circuits are modified in accordance with said predetermined logical relationship.

65. The device according to claim 64, wherein said initial data are loaded from at least one input line.

66. The device according to claim 63, wherein said plurality of programming circuits simultaneously determine said actual written states of said memory cells.

67. The device according to claim 63, wherein said data stored in said plurality of programming circuits are modified simultaneously in accordance with said predetermined logical relationship.

68. The device according to claim 63, wherein said programming circuits include means for selectively changing voltages of said bit lines according to said data stored in said programming circuits.

69. The device according to claim 68, wherein said voltages of said bit lines are changed selectively and simultaneously by said means for selectively changing voltages of said bit lines.

70. The device according to claim 63, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to said respective of said memory cells are continued until each memory cell is sufficiently written.

71. The device according to claim 63, wherein modifying of said data stored in said programming circuits and applying said write voltages according to said data stored in said programming circuits are repeated during a limited number of cycles.

72. The device according to claim 63, wherein said programming circuits are arranged on a semiconductor substrate.

73. The device according to claim 72, wherein said programming circuits are arranged adjacent to said memory cell array.

74. The device according to claim 63, wherein each of said programming circuits is connected to a respective one of said bit lines.

75. The device according to claim 63, further comprising a verify-termination detector for detecting whether or not all of said memory cells are sufficiently written in accordance with the modified data in said programming circuits based on said predetermined logical relationship.

76. The device according to claim 75, wherein said verify-termination detector is arranged on a semiconductor substrate.

77. The device according to claim 63, in which said plurality of programming circuits selectively modify said stored data based on said predetermined logical relationship between the determined actual written states of said memory cells after application of write voltages thereto and

the actual data stored by said plurality of programing circuits prior to application of said write voltages.

78. The device according to claim 63, wherein said plurality of programming circuits simultaneously apply said write voltages to said part of said memory cells.

79. A non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion;

a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, said data being initially set to initial data which are loaded from at least one input line, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, said write voltages applied only to memory cells which are not sufficiently written to produce charge storage in the charge storage portion of each respective insufficiently written memory cell.

80. A system including a non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion; and

a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, said data being initially set to initial data which are loaded from at least one input line, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected

according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, thereby applying said write voltages only to memory cells which are not sufficiently written to produce charge storage in the charge storage portion of each respective insufficiently written memory cell.

81. The system according to claim 80, wherein said plurality of programming circuits simultaneously determine said actual written states of said memory cells.

82. The system according to claim 80, wherein said data stored in said programming circuits are modified simultaneously in accordance with said predetermined logical relationship.

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83. The system according to claim 80, wherein said programming circuits include means for selectively changing voltages of said bit lines according to said data stored in said programming circuits.

84. The system according to claim 83, wherein said voltages of said bit lines are changed simultaneously by said means for selectively changing voltages of said bit lines.

85. The system according to claim 80, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to said respective of said memory cells are continued until each memory cell is sufficiently written.

86. The system according to claim 80, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to said respective of said memory cells are repeated during a limited number of cycles.

87. The system according to claim 80, wherein said programming circuits are arranged on semiconductor substrate.